Remarks

With the Advisory Action, the instant Office Action dated February 18, 2010 is understood to now carry the following rejections: claims 1, 3 and 4 stand rejected under 35 U.S.C. § 103(a) over Dally (U.S. Patent No. 6,192,384) in view of Garde (U.S. Patent No. 6,510,510); and claims 2 and 5-7 stand rejected under 35 U.S.C. § 103(a) over the '384 and '510 references in further view of Fisher (U.S. Patent No. 6,026,479). Applicant traverses all of the rejections and, unless stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully maintains the traversal of the § 103(a) rejections because the cited '384 reference either alone or in combination with the '510 reference lacks correspondence to the claimed invention. As explained below, the Advisory Action's reasons for maintaining the rejections are technically flawed and improper in view of the requirements for a § 103 rejection. Neither of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.,* a second set of issue slots that have holdable registers on the single data input path of an input routing network and that do not have holdable registers on the multiple data output paths of the input routing network. The Advisory Action supposes that the skilled artisan would somehow combine these latches (132 of Garde) on some slots as taught by Dally. However, the Advisory Action and the Final Office Action fail to specify any slots of Dally that would be so modified. There would be no reason to use the latches of Garde with the clusters 18 of Dally (*see* Advisory Action) because Dally already provides circuits for storing such data as it passes to and from the clusters 18 (*see* '384 reference at Col. 4:7-17). Therefore, the Final Office Action fails to comply with the M.P.E.P. by failing to articulate anything enabled or understood. The Examiner's rationale for maintaining the rejection clearly ignores the vast majority of Applicant's arguments presented in response to the Final Office Action and appears to present nothing more than the improper argument that the combination in "some" form would be "obvious to try". The impropriety of this rationale is clearly explained by the Federal Circuit's *Kubin* decision (*In re Kubin*, 561 F.3d 1351 (Fed. Cir. 2009)). The *Kubin* court further confirmed the court's holding in *O'Farrell*, as reinvigorated by the court in *KSR*, that the cited references should contain "detailed enabling methodology for practicing the claimed invention, a suggestion to modify the prior

art to practice the claimed invention, and evidence suggesting that it would be successful." (*In re O'Farrell,* 853 F.2d 894 (Fed. Cir. 1988)). Because neither reference teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence to the claimed invention. As such, the § 103(a) rejections fail.

Applicant submits that the Applicant's previously presented remarks, as presented again below, overcome the rationale and rejections. The Examiner is obligated to address each of these arguments in substance. *See* M.P.E.P § 707.07(f). More specifically, aspects of the claimed invention are directed to particular placements of holdable registers within a multi-issue processor. As discussed in Applicant's disclosure, multi-issue processors contain multiple functional units. Depending upon the current instruction, one or more of the functional units might not be used each cycle. Thus, one aspect of the invention uses a first set of issue slots that have holdable registers located at the input of the functional units (*see, e.g.,* Figure 2). Thus, when a functional unit is not used, the input remains constant, thereby reducing power consumption of the functional unit. Other aspects of the present invention recognize that when an interrupt event occurs, the presence of such holdable registers means that a large amount of data needs to be stored before the interrupt event can be processed. Thus, a second set of issue slots have holdable registers implemented before a routing network (*see, e.g.,* Figure 3) and do not have holdable registers located at the input of each of the functional units. The routing network provides multiple data outputs for a single data input and therefore, the total number of registers is less when placed before the routing network. The second set of holdable registers can, for example, be used in connection with an issue slot that is associated with interrupts (*see, e.g.,* claim 5).

Turning now to the cited references, neither the '384 reference nor the '510 reference teach issue slots that have holdable registers on the single data input path of an input routing network and that do not have holdable registers on the multiple data output paths of the input routing network, as in the claimed invention. For example, the '384 reference teaches that each of ALU clusters 18 (*i.e.,* the asserted issue slots) uses the same configuration of buffers 28 (*i.e.,* the asserted holdable registers) with a buffer 28 being located on each output of cross point switch 30 (*i.e.,* the asserted outputs of the input routing network) in each of the ALU clusters 18. *See, e.g.,* Figures 1 and 2. Thus, the '384 reference does not teach issue slots that do not have holdable registers on the multiple data

output paths of the input routing network as claimed. Applicant submits that the '510 reference also fails to teach such aspects of the claimed invention. Instead, the '510 reference teaches that each of computational blocks 12 and 14 (*i.e.*, the asserted issue slots) uses the same configuration of latches (*i.e.*, the asserted holdable registers) with a latch 132 being located on the input to buses 110 and 112 and latches 160 and 165 located on the outputs of the buses 110 and 112 (*i.e.*, the asserted outputs of the input routing network) in each of the computational blocks 12 and 14. *See, e.g.*, Figures 1 and 2. As such, the '384 reference also does not teach issue slots that do not have holdable registers on the multiple data output paths of the input routing network as claimed. Instead, the '384 and '510 references both teach that each of the asserted issue slots have holdable registers on the asserted outputs of the input routing network. Therefore, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence to the claimed invention.

Moreover, Applicant submits that the '384 reference teaches away from a modification that would remove the buffers (local register files) 28 from some of the ALU clusters 18. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('384) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). In this instance, the '384 reference teaches that the ALU clusters 18 use the local register files 28 to store intermediate results produced during computations within the cluster so they do not need to re-circulate through the stream register 14. *See, e.g.*, Col. 4:7-17. Consistent with the purpose of the '384 reference, the use of the local register files 28 provides a tiered storage architecture thereby reducing bandwidth demands on the stream register file. *See, e.g.*, Col. 2:24-27 and Col. 2:46-51. Thus, removing the local register files 28 from some of the ALU clusters 18 would undermine the operation and the purpose of the '384 reference because the '384 reference would no longer be able to make use of the local register files 28 in the ALU clusters 18 from which they are removed as consistent with the teachings of the '384

reference. Applicant submits that removing the local register files 28 from some of the ALU clusters 18 would also change the principal of operation of the '384 reference because the local register files 28 would no longer be available to provide a tiered storage architecture as in the '384 reference. *See, e.g.,* M.P.E.P. § 2143.01 ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."). Accordingly, the '384 reference teaches away from such a modification and the rejections cannot be maintained.

In addition, Applicant submits that the Examiner's assertion in the instant Office Action that "a reference only 'teaches away' when it states that something cannot be done" is misleading at best. Applicant has reviewed the *In re Gurley* case, purported by the Examiner to support the Examiner's assertion, and Applicant can find no support for the Examiner's contention that a reference "only" teaches away in such a limited instance. *See In re Gurley* 27 F.3d 551, 553 (Fed. Cir. 1994). Applicant submits that relevant law, including the recent *KSR* decision by the Supreme Court, and the M.P.E.P. are clear that a reference teaches away from a modification in situations other than the limited instance asserted by the Examiner. As such, the Examiner has failed to offer any substantive rebuttal of the evidence of record that the '384 reference teaches away from the Examiner's proposed modification. Accordingly, Applicant submits that the record stands uncontroverted regarding the impropriety of the Examiner's proposed modification of the '384 reference

In view of the above, the § 103(a) rejections are improper and Applicant requests that they be withdrawn.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Schaeffer, of NXP Corporation at (408) 474-9068 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

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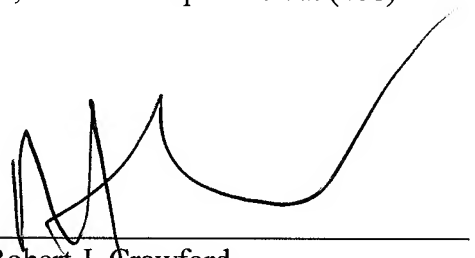
By: 

Robert J. Crawford
Reg. No.: 32,122
651-686-6633 x2300
(NXPS.305PA)